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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/694,842	10/29/2003	Joung-Hyun Yeo	Q77421	2497

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EXAMINER

NGUYEN, JIMMY H

ART UNIT	PAPER NUMBER
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2629

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	03/02/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary

Application No.

10/694,842

Applicant(s)

YEO, JOUNG-HYUN

Examiner

Jimmy H. Nguyen

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 16 January 2007.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1,3-11 and 13-18 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1,3-11 and 13-18 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on _____ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.
- Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
- Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☐ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date _____
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____

DETAILED ACTION

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 1/16/2007 has been entered. Claims 1, 3-11 and 13-18 are currently pending in the application. An action follows below:

Allowable Subject Matter

2. The indicated allowability of claims 2-10 and 12 in the Office Action dated 10/13/2006 is withdrawn. Rejections follow.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

4. Claims 1, 3-11, and 13-18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Toda et al. (US 6,650,307 B1), hereinafter Toda, and further in view of Tomio et al. (US 5,745,085), hereinafter Tomio.

As to claims 1, 11, 14, 17 and 18, the claimed invention reads on the Toda reference as follows: Akiyama discloses a plasma display apparatus with low power consumption and high speed response (see Fig. 8 and Abstract) comprising a **plasma display panel (1)** driven by a discharge sustain voltage in the form of pulses (best seen Fig. 2); **an analog-digital converter (a**

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circuit comprising an A/D converter for receiving an analog image signal; see col. 1, lines 45-51 and col. 5, lines 39-43; and a gain control circuit 21; see Fig. 8) digitizing an image signal and producing a digitized image signal; **a plasma display panel drive unit** (an unit comprising at least elements 2-4, 12 and 13, see Fig. 8) converting the digitized image signal into scanning pulses and data pulses for driving the plasma display panel and outputting the scanning and data pulses to the plasma display panel; **a power supply unit** (a portion of a power source 5 for generating signals provided to drivers 2 and 3 as shown in Fig. 8) supplying the discharge sustain voltage to the plasma display panel drive unit; and **a controlling unit** (a unit comprising elements 22, 23 and a portion of a power source 5 which detects, determines, and provides the voltage and current values to a power control circuit 23, see Fig. 8 and col. 6, lines 3-11), which includes a voltage sensing unit (a portion of a power source 5 which detects, determines, and provides the voltage and current values to a power control circuit, see Fig. 8 and col. 6, lines 3-11) sensing the discharge sustain voltage and discharge current during the sustaining discharge period (see col. 3, lines 36-44) and a power control circuit (23) calculating the power consumption based on the detected (sensed) voltage and current to determine the gain coefficient for adjusting an output gain of the analog-digital converter in response to a variation of the discharge sustain voltage of the power supply unit (see Fig. 8; col. 6, lines 3-11). Toda teaches the power control circuit (23) further comprising a power comparison unit comparing the calculated power consumption with a predetermined limit value PM and a gain adjusting unit outputting the gain coefficient to adjust the output gain of the analog-digital converter depending on the comparison results (see col. 6, lines 15-65). In other words, Toda teaches a power comparison unit instead of a voltage comparison unit as claimed. Accordingly, Toda discloses all

the claimed limitations of these claims except that Toda does not expressly teach a voltage comparison unit and a scaler, as presently claimed.

However, Official Notice is taken that both the concept and the advantages of providing a scaler in the plasma display apparatus, for processing or converting the digitized image signal to an image size appropriate to the plasma display panel, are well-known and expected in the art. It would have been obvious to one of ordinary skill in the art at the time of the invention was made to provide the scaler in the plasma display apparatus of Toda, because this would allow the user to view an input image signal having any size, on the display apparatus.

Further, regarding to the claimed voltage comparison unit, Tomio discloses a related plasma display apparatus (see Fig. 1) comprising a controlling unit (a unit including elements 37, 39, 40; see Fig. 1), which includes a voltage sensing unit (39) (see Figs. 1 and 3) sensing the variation of the discharge sustain voltage and outputting a sensed voltage and a voltage comparison unit (40) comparing the sensed voltage from the voltage sensing unit with a predetermined voltage and outputting comparison results (see Fig. 1; col. 10, lines 1-16). Tomio further teaches that the benefit of detecting and comparing the current and the discharge voltage separately is “to provide a display panel of a lower power consumption type which is not affected by the display rate, as well as to provide a display panel capable of displaying an image while maintaining stable brightness and suppressing changes in the brightness regardless of a change in the display rate or a change in the setpoint display voltage V_s , by improving the aforementioned defects inherent in the prior art” (see col. 5, lines 42-49). See col. 6, lines 4-50. Therefore, it would have been obvious to a person of ordinary skill in the art at the time of the invention was made to modify the controlling unit of Toda to compare the current and the

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discharge voltage separately, rather than to compare the power consumption, in view of the teaching in the Tomio reference, because this would provide a display panel of a lower power consumption type which is not affected by the display rate, as well as to provide a display panel capable of displaying an image while maintaining stable brightness and suppressing changes in the brightness regardless of a change in the display rate or a change in the setpoint display voltage V_s , as taught by the Tomio reference (see col. 5, lines 42-49).

As to claim 13, Toda expressly teaches that when a luminance level of the digitized image signal increases, the power consumption and the gain of the input image signal are reduced (see col. 7, lines 8-15), thereby reducing the discharge sustain voltage.

As to claims 15 and 16, as discussed in the rejection to claim 11 above, Toda discloses all the claimed limitations of this claim except that Toda does not expressly teach a decoder unit receiving an externally inputted image signal, converting it into the image signal and outputting the image signal, and outputting the image signal to the analog-digital converter for digitizing, as presently claimed. However, Official Notice is taken that both the concept and the advantages of providing a decoder unit in the plasma display apparatus, for receiving an externally inputted image signal, converting it into the image signal and outputting the image signal, and outputting the image signal to the analog-digital converter for digitizing, are well-known and expected in the art. Therefore, it would have been obvious to one of ordinary skill in the art at the time of the invention was made to provide the decoder unit in the plasma display apparatus of Toda, because this would allow the display apparatus to receive a plurality of externally inputted image signals

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from a plurality of image sources, thereby allowing a user to view a desired image on the display.

As to claim 3, Tomio teaches the voltage sensing unit (39) includes a first resistor (R5) and a second resistor (R6) connected in series between the discharge sustain voltage (Vs) and a ground (see Fig. 3).

As to claim 4, as discussed in the rejection to claim 1 above, Tomio discloses a voltage comparison unit (40) comparing the sensed voltage from the voltage sensing unit with a predetermined voltage and outputting comparison results (see Fig. 1; col. 10, lines 1-16). Tomio's voltage comparison unit does not comprise an operational amplifier, a third resistor, and a fourth resistor, as presently claimed. However, Official Notice is taken that both the concept and the advantages of constructing a voltage comparison unit by using analog elements, an analog operational amplifier inputted with a predetermined voltage at its first input terminal, a third resistor connected between a node commonly connected to the first resistor and the second resistor and a second input terminal of the operational amplifier, and a fourth resistor connected between an output terminal of the operational amplifier and an input terminal of another unit are well-known and expected in the art. It would have been obvious to replace the comparison unit (40) of Tomio with the known analog voltage comparison unit because this would reduce the high cost of the voltage comparison unit using the MPU (35), memory (42), a selector (38), and a converter (36).

As to claim 5, as discussed in the rejection to claim 1 above, Toda teaches the power control circuit (23) comprising an inherent data storage unit storing the gain coefficients (i.e., a gain value of the analog-digital converter) and an inherent microcomputer for supplying a predetermined power limit value PM for comparison (see col. 6, lines 15-65). Accordingly, Toda in view of Tomio discloses the limitations of this claim.

As to claim 6, see the rejection to claim 4 above.

As to claim 7, see the rejection to claim 5 above.

As to claim 8, see the rejection to claim 13 above.

As to claim 9, Toda expressly teaches that when a luminance level of the digitized image signal increases, the power consumption and the gain of the input image signal are reduced (see col. 7, lines 8-15).

As to claim 10, see the rejection to claim 14 above.

Conclusion

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jimmy H. Nguyen whose telephone number is 571-272-7675. The examiner can normally be reached on Monday - Friday, 6:30 a.m. - 3:00 p.m..

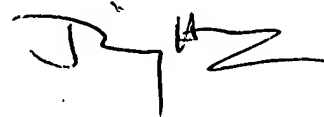
If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Bipin Shalwala can be reached at 571-272-7681. The fax phone number for the organization where this application or proceeding is assigned is (571) 273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished

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applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

JHN
March 1, 2007



Jimmy H. Nguyen
Primary Examiner
Technology Division: 2629